

Figure 1

Cross-section of a trenched DMOS power transistor cell (prior art, /1,2/).

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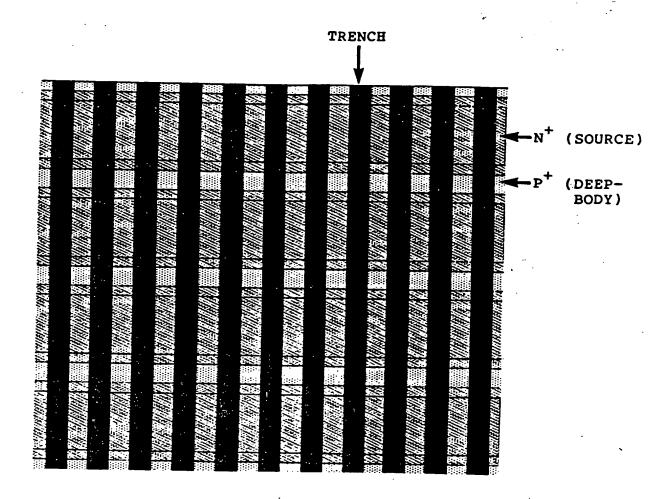


Figure 2,a

"Open-cell" implementation of a trenched DMOS power transistor (CALMA hard copy, active region).

Siliconix, Inc., 1987.

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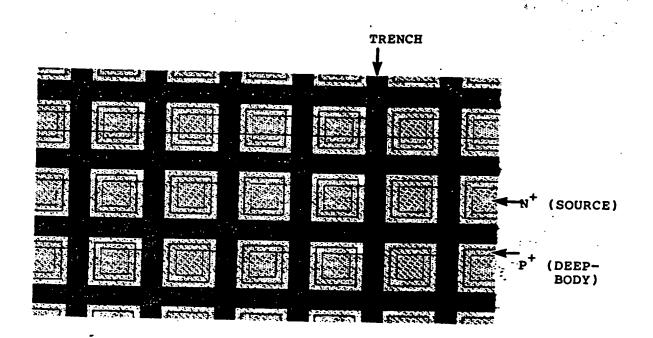
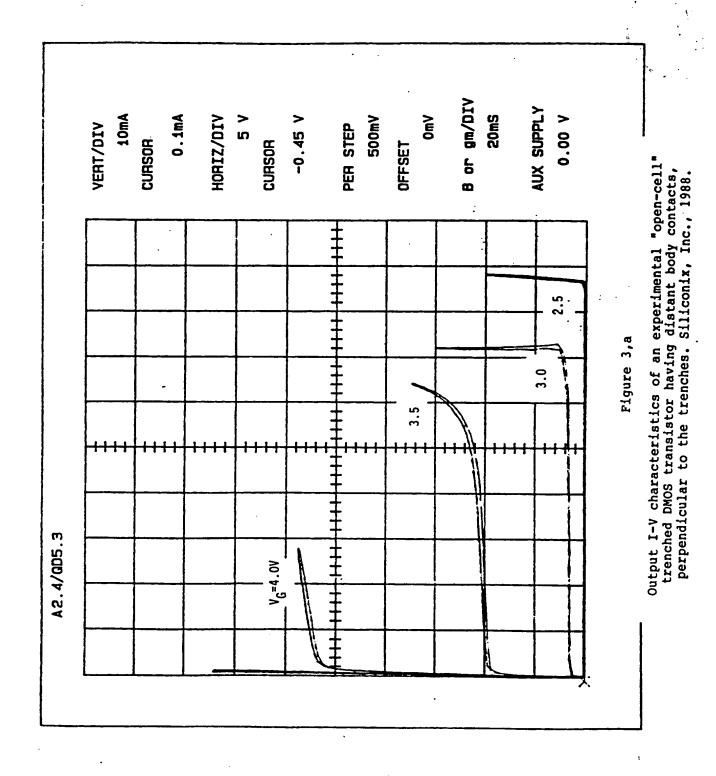


Figure 2,b

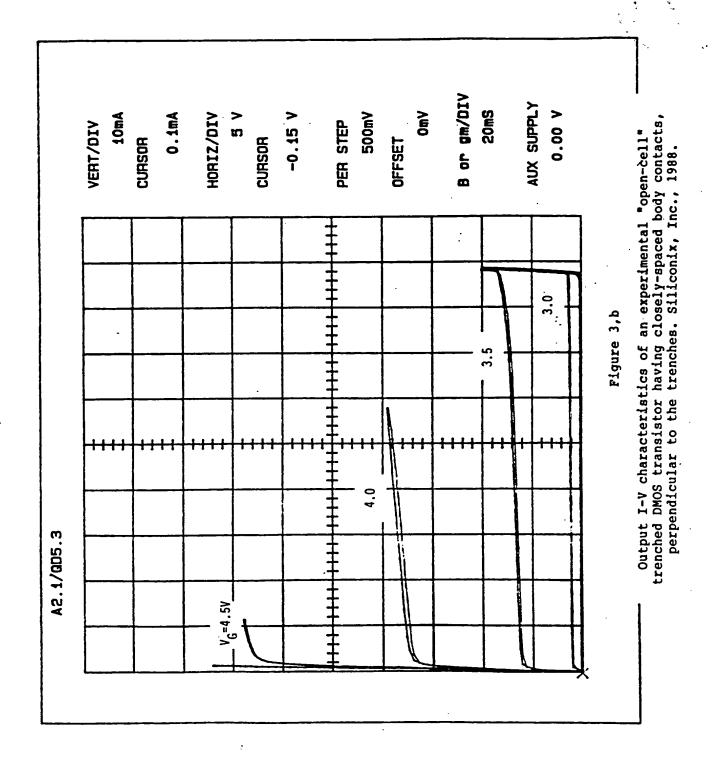
"Closed-cell" implementation of a trenched DMOS power transistor (CALMA hard copy, active region). Siliconix, Inc., 1987.

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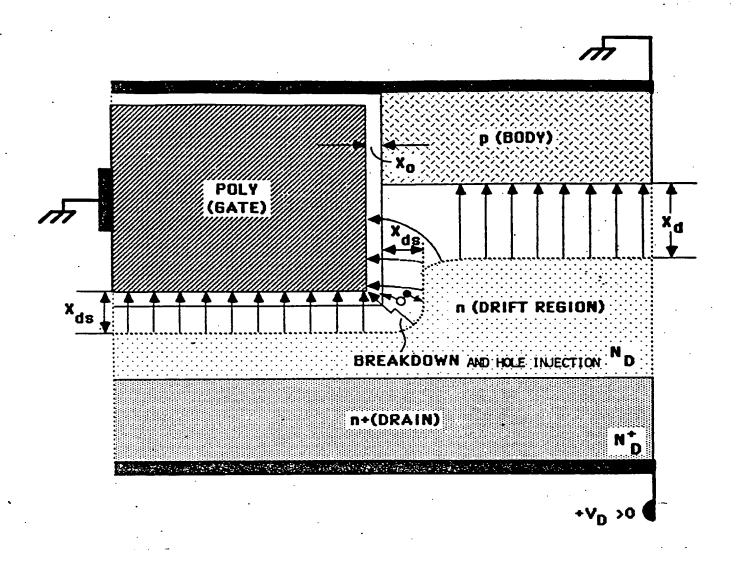


Figure 4

Qualitative description of the electric-field structure in a trenched DMOS transistor having no deep-body profile provision. BVDSS biasing, source junction omitted.

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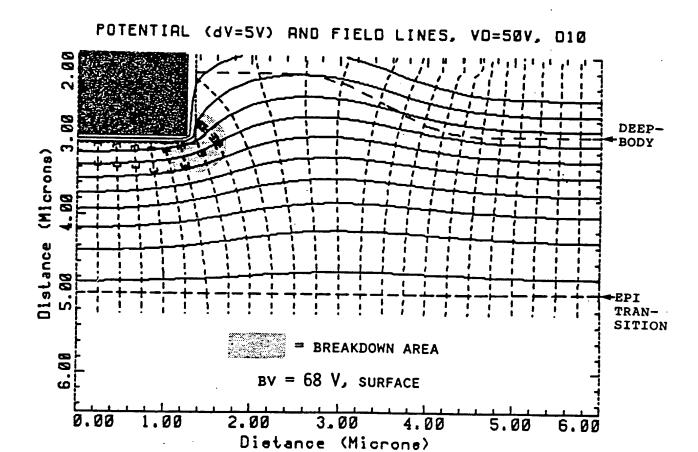


Figure 5

2-D computer simulation of the BVDSS operation of a trenched DMOS transistor having the deep body junction shallower than the trench.

Drain breakdown takes place beneath the trench surface.

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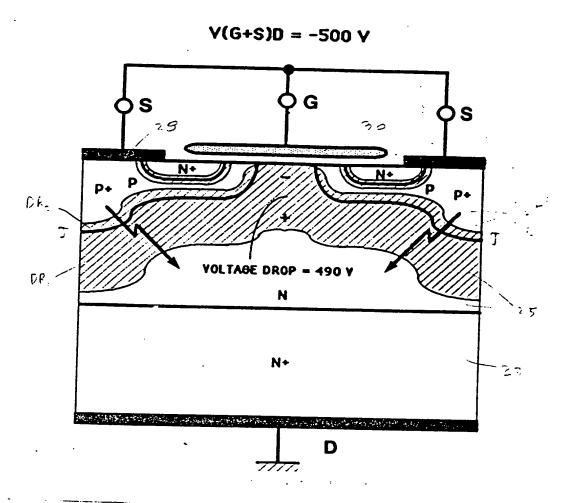
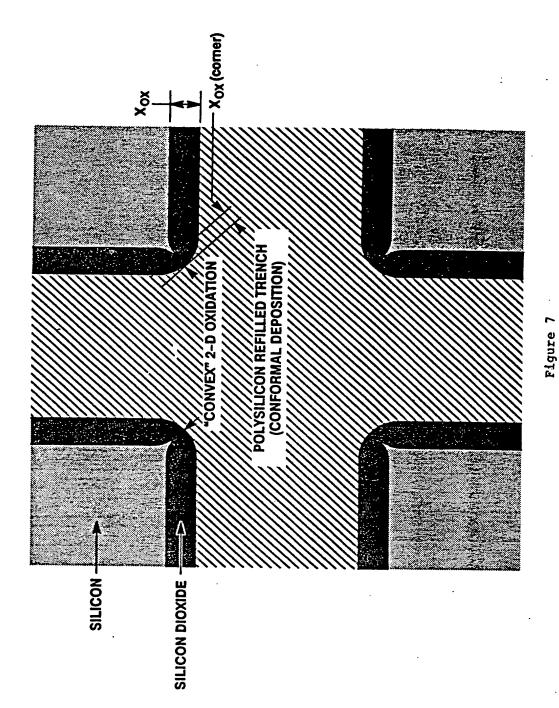


Figure 6

Junction and depletion-region topology of a planar DMOS transistor biased in the BVDSS condition.

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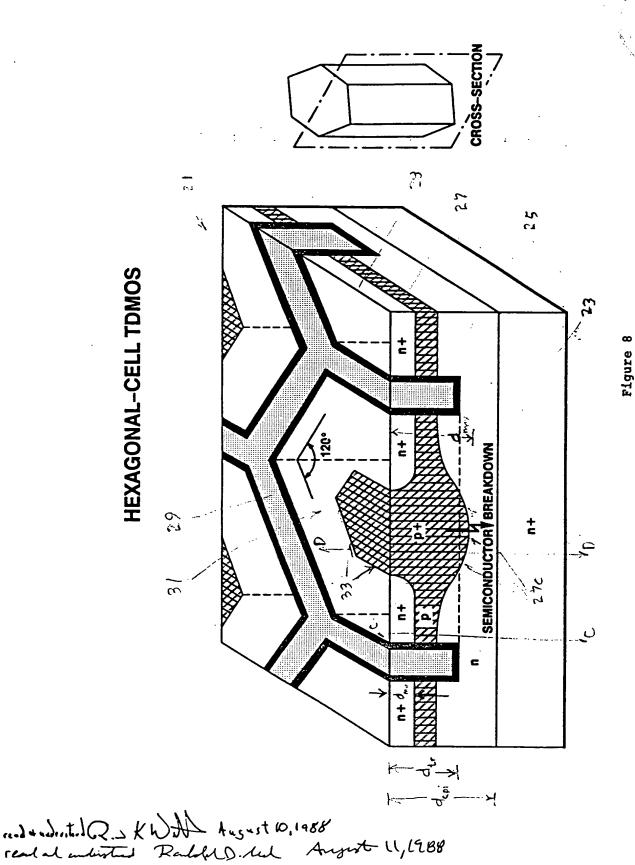
2-D OXIDATION SQUARE-CELL DESIGN



Qualitative description of the oxide profile at a rectangular trench intersection.

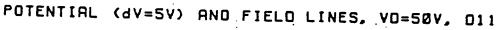
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3-D representation of the optimized trenched DMOS transistor cell proposed in this Patent Application.

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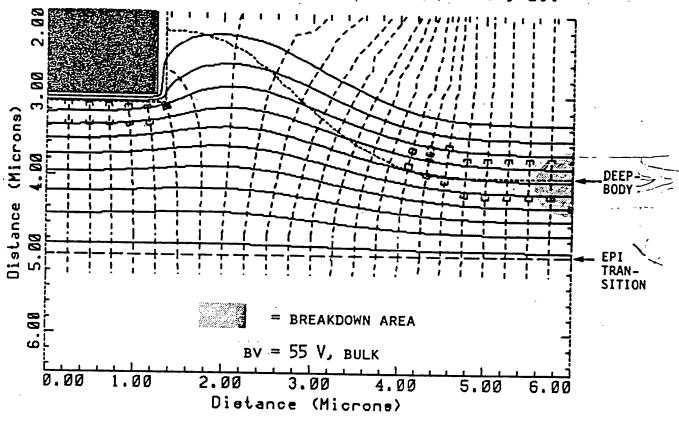


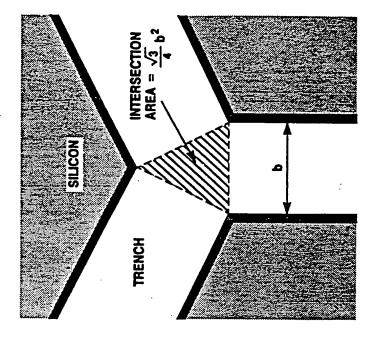
Figure 9

2-D computer simulation of the BVDSS operation of a trenched DMOS transistor having the deep body junction deeper than the trench.

Drain breakdown takes place in the bulk.

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"BLACK SILICON" COMPARISON



INTERSECTION AREA = b^2

TRENCH

SILICON

HEXAGONAL CELLS

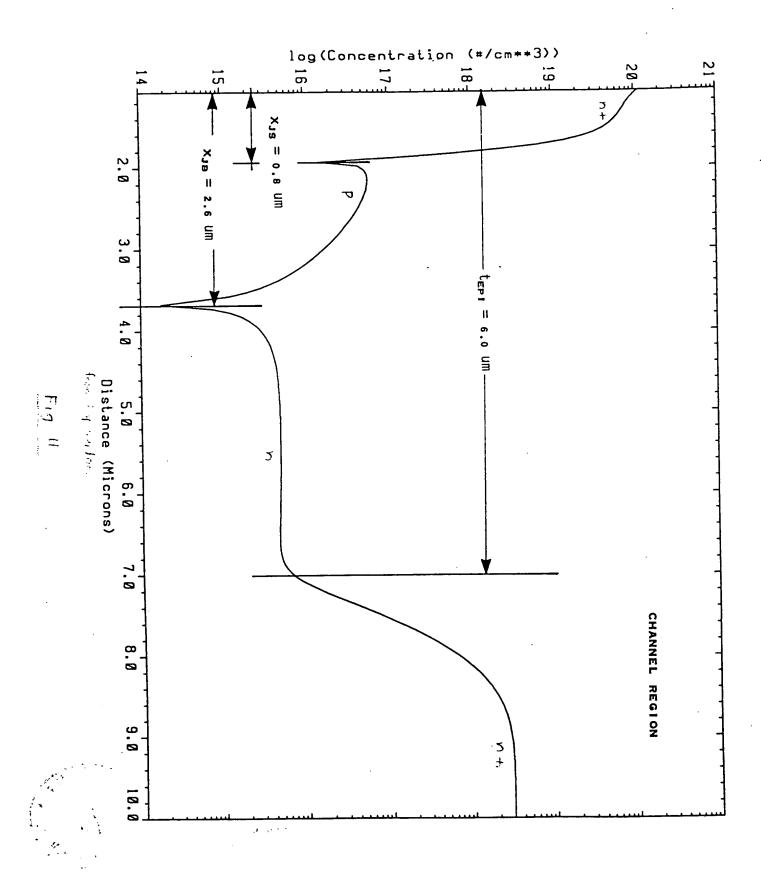
SQUARE CELLS

Figure 10

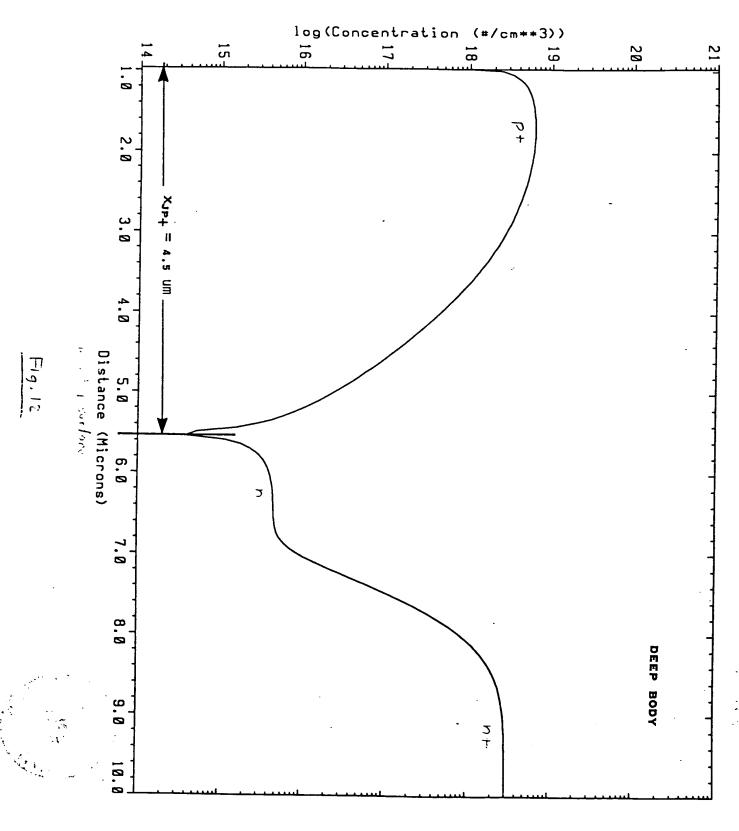
Comparison of the "black silicon" areas at trench intersections: square cell (left) versus hexagonal cell (right).

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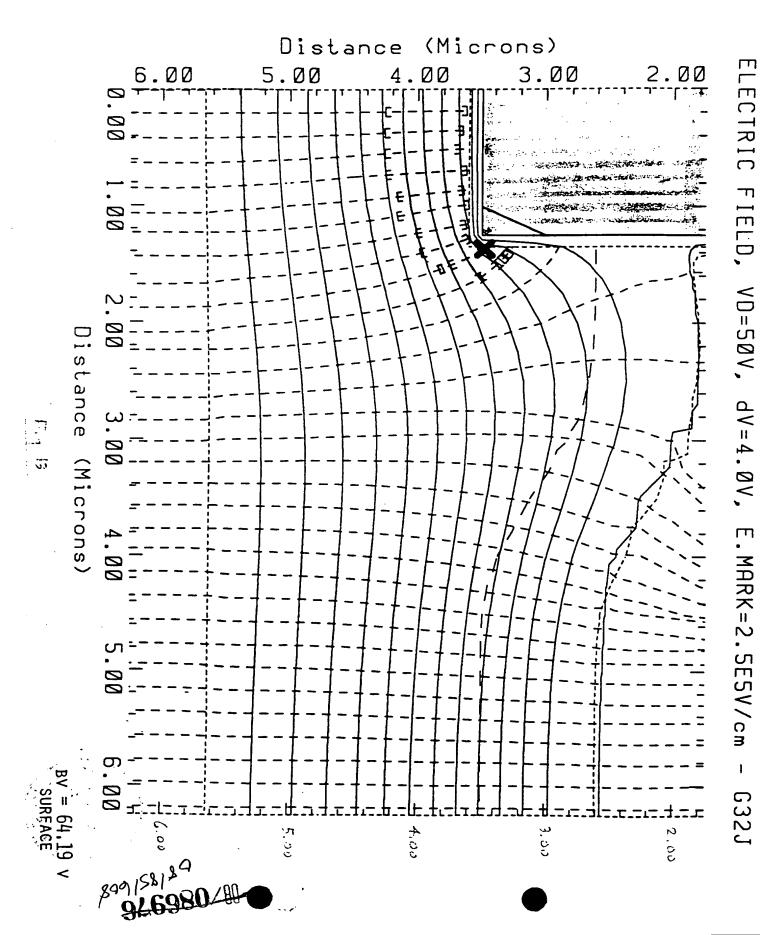
"BLACK SILICON"

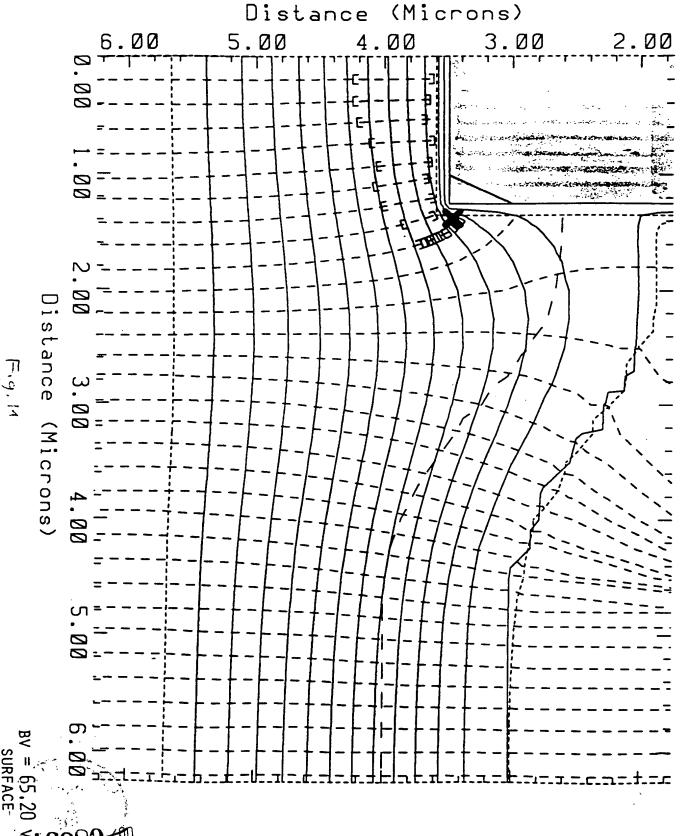


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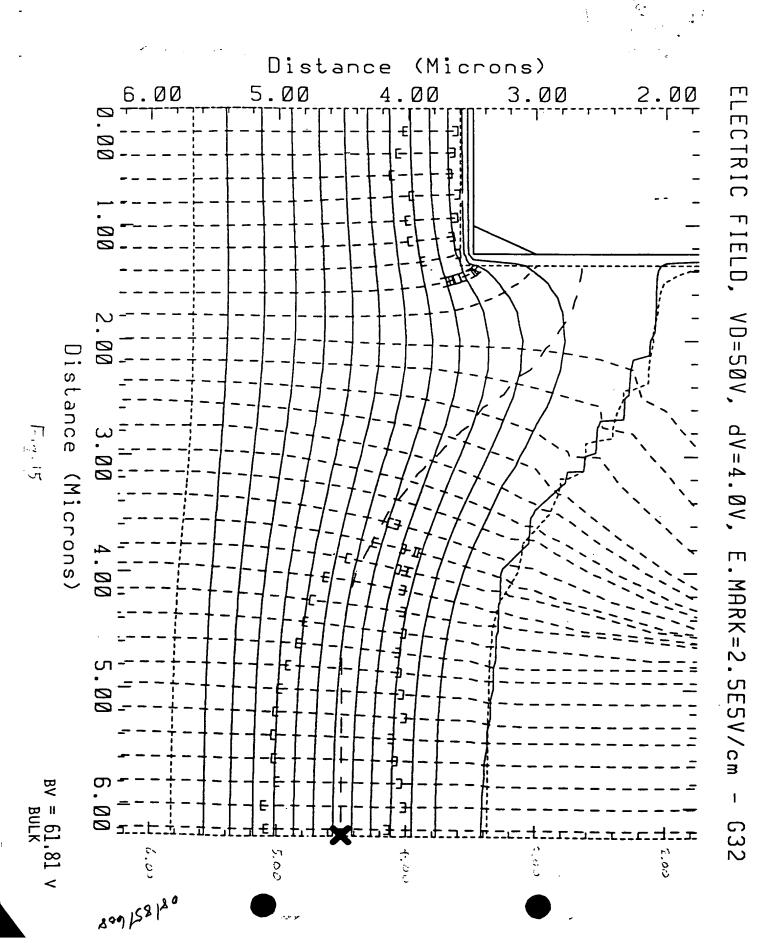
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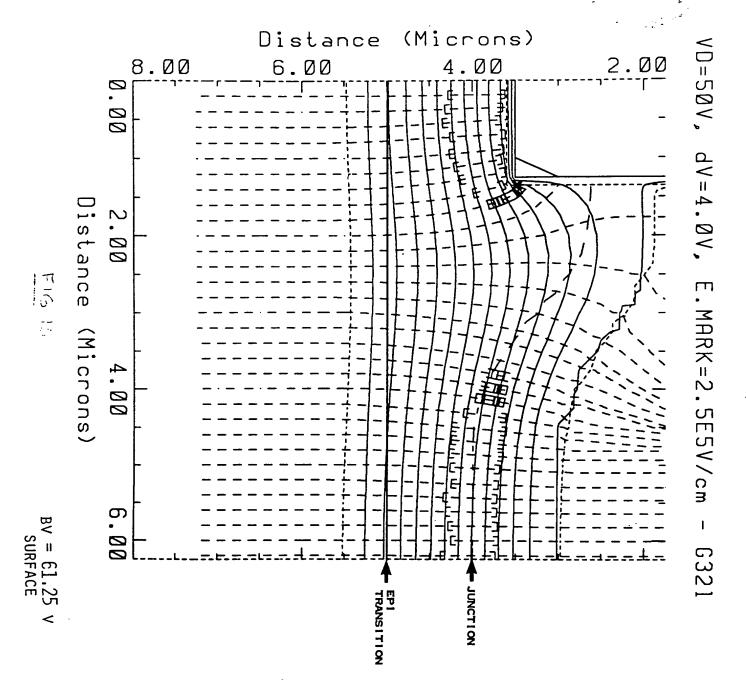




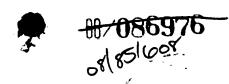
FIELD, VD=50V, dV=4.0V, E.MARK=2.5E5V/cm G32k

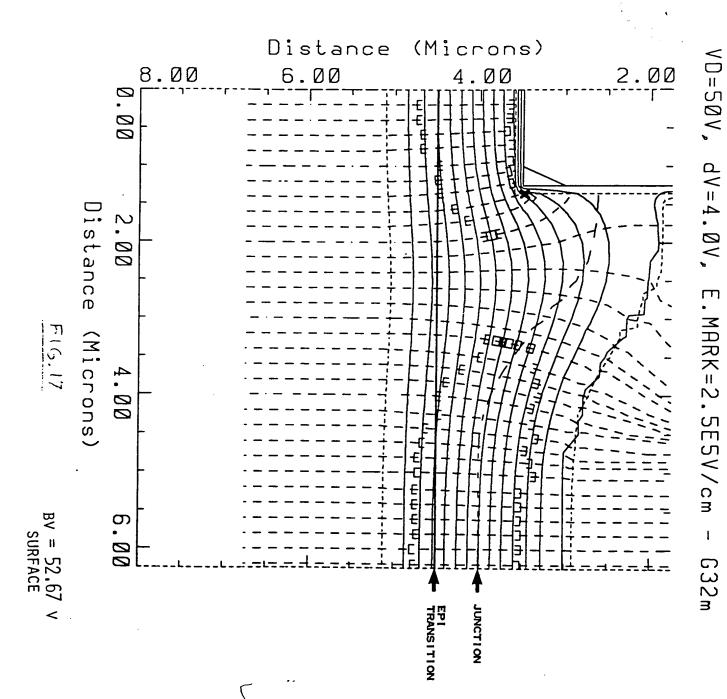
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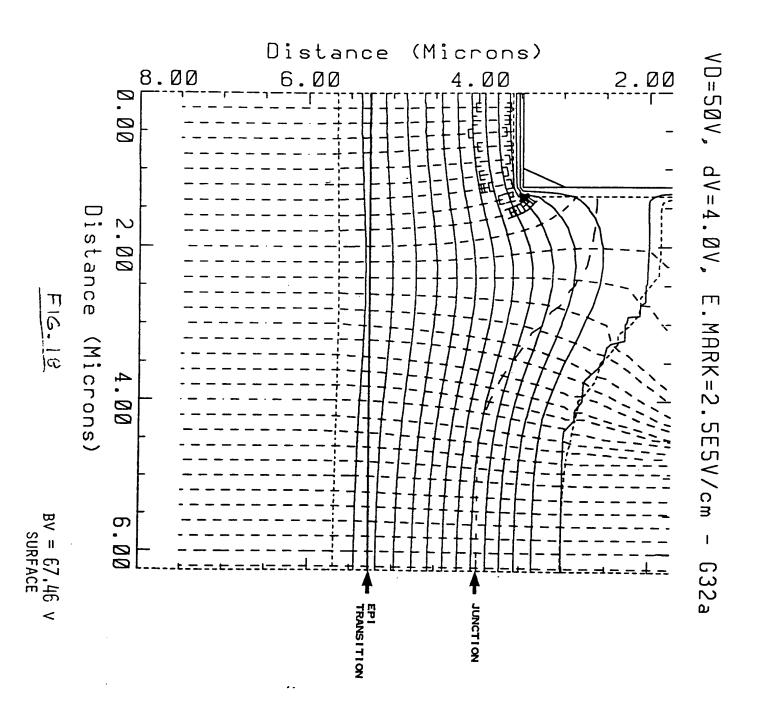


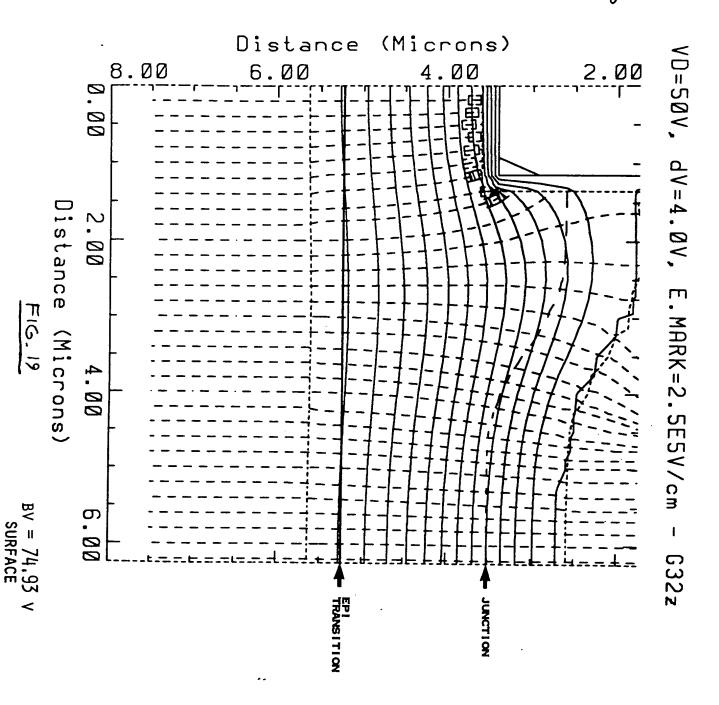


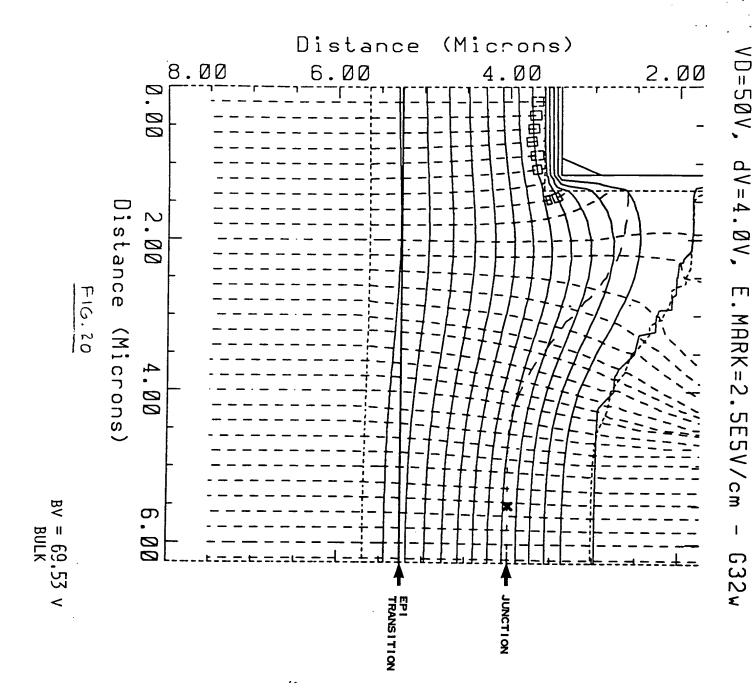
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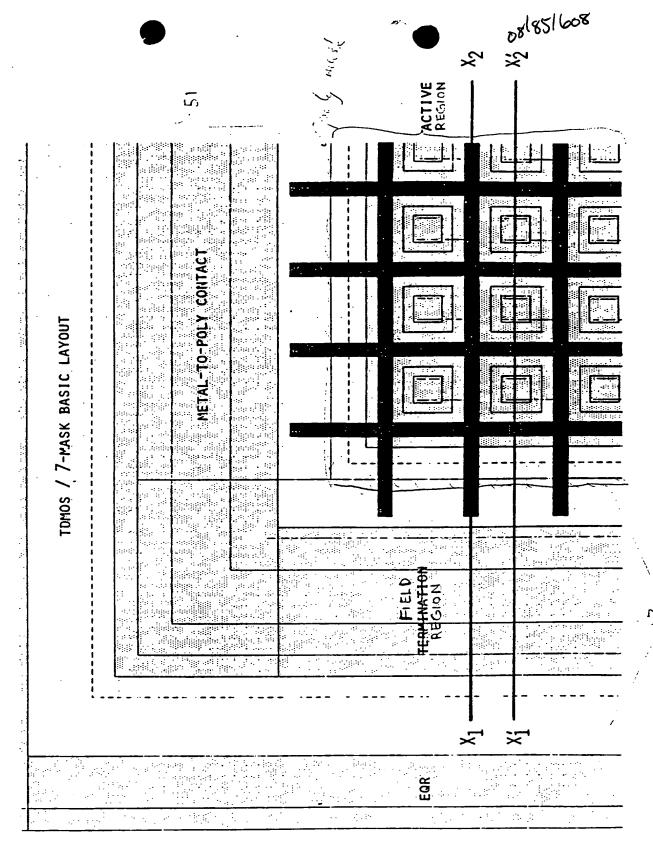


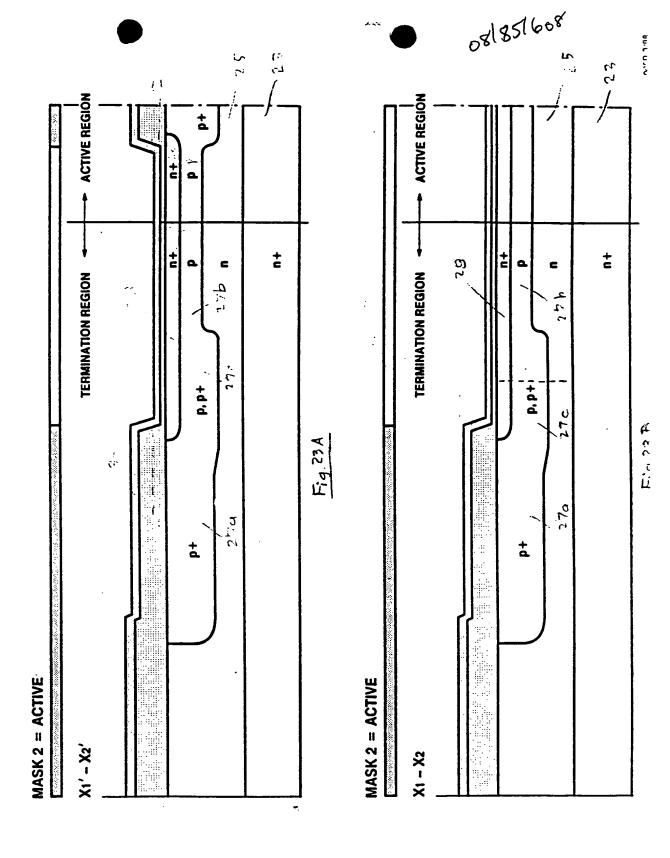
Fig. 21

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081851608 23 2 123 7-MASK TDMOS-PROCESSING BLOCK 1
PPOST-EPI OXIDATION - MASK 1 = DEEP BODY - BORON IMPLANT & DIFFUSION / OXIDATION -**ACTIVE REGIÓN** ◆ ACTIVE REGIÓN ŧ **+** ţ = = **TERMINATION REGION TERMINATION REGION** F19.22A p td 11.32月 279 MASK 1 = DEEP BODY MASK 1 = DEEP BODY X1' - X2' X1 - X2 n/n + EPI

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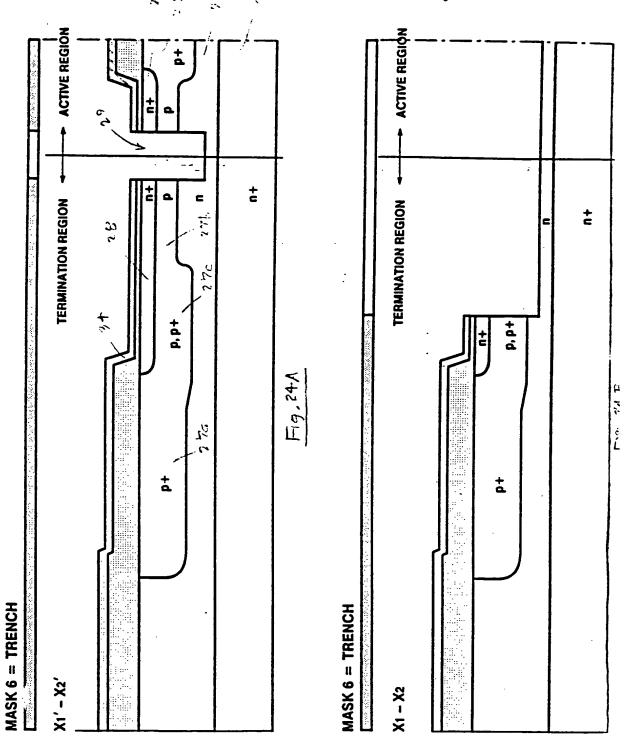
MASK 2 = ACTIVE MBORON IMPLANT & DIFFUSION / OXIDATION MARSENIC IMPLANT & DIFFUSION / OXIDATION MALTO DEPOSITION 7-MASK TDMOS-PROCESSING BLOCK 2



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7-MASK TDMOS—PROCESSING BLOCK 3

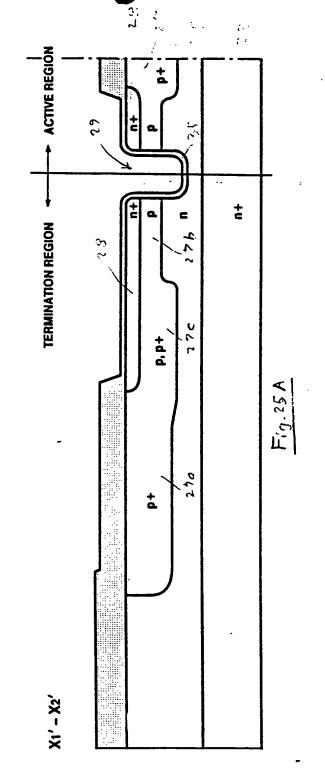
MASK 6 = TRENCH TRENCH DRY ETCHING

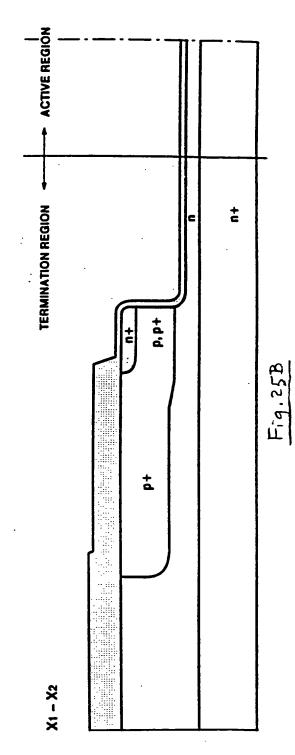




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08/82/ 608 621 - ACTIVE REGIÓN **ACTIVE REGIÓN + TERMINATION REGION** ÷ TERMINATION REGION 96 بر در p.p+ F19, 26B F19.26A 3 '4 C td t X1' - X2' X1 - X2

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► OXIDATION (ETCH STOP)

7-MASK TDMOS-PROCESSING BLOCK 5

FIRST POLY DEPOSITION & PHOSPHORUS DOPING

ACTIVE REGIÓN ŧ TERMINATION REGION 28 p. p+ F.g. 27A 800 td X1' - X2'

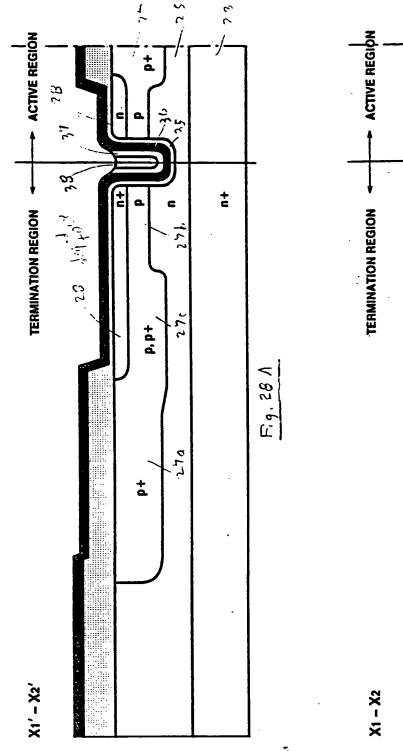
ACTIVE REGIÓN + TERMINATION REGION p.p+ F19.27B ŧ X1 - X2

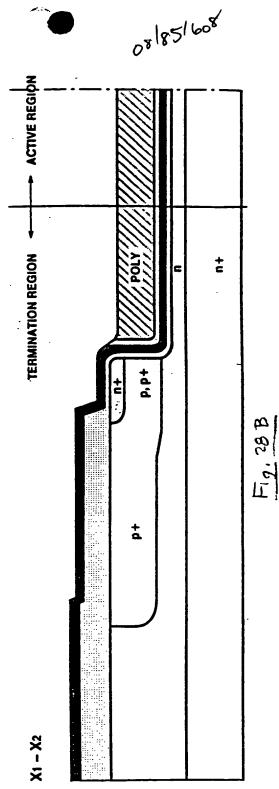
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SECOND (UNDOPED) POLY DEPOSITION

7-MASK TDMOS-PROCESSING BLOCK 6

7-MASK TDMOS – PROCESSING BLOCK 7





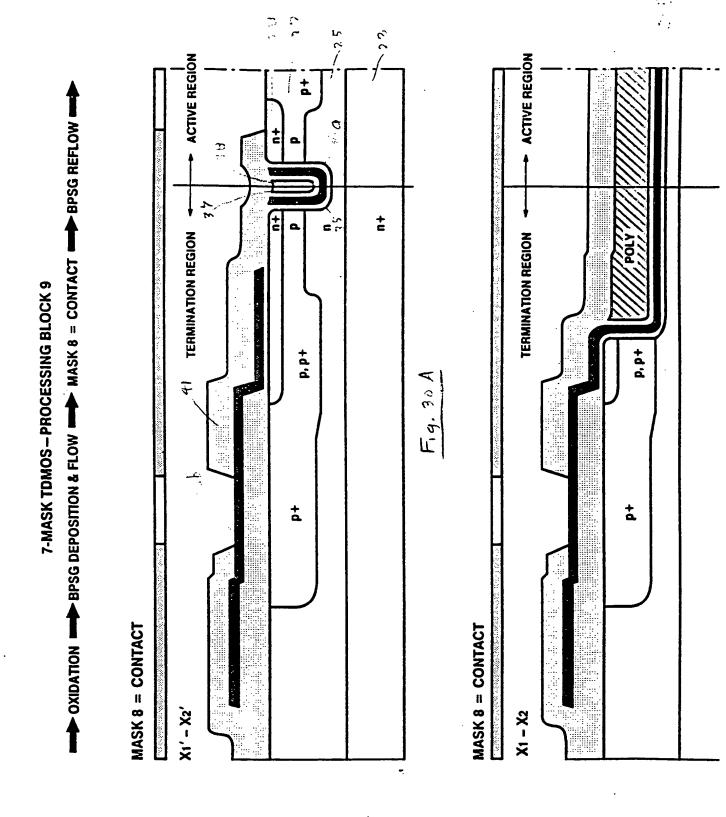
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04/85/608 **ACTIVE REGIÓN** ACTIVE REGIÓN t **TERMINATION REGION TERMINATION REGION +** \$ p, p+ F.g. 29A F19.29 B t L MASK 7 = POLY MASK 7 = POLY X1' - X2' X1 - 12

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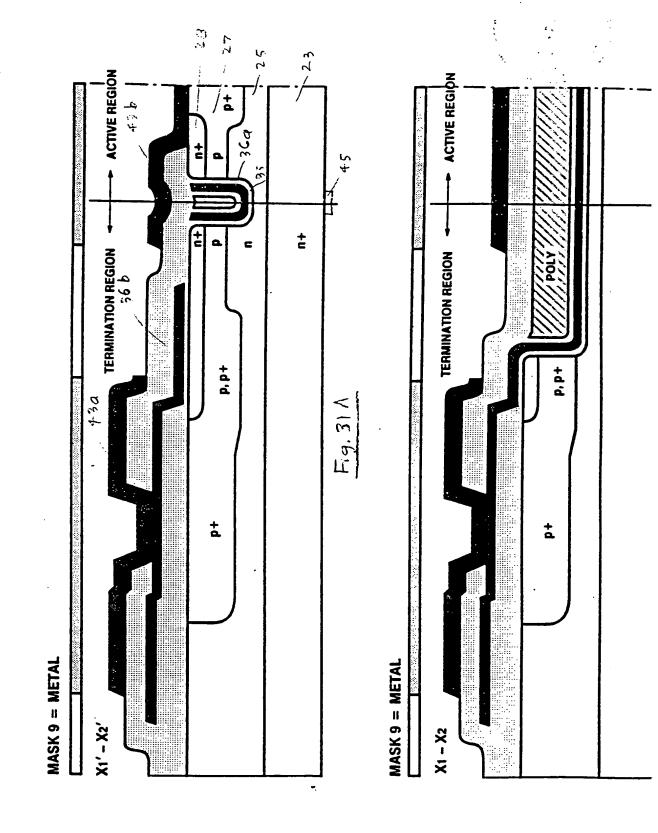
7-MASK TDMOS-PROCESSING BLOCK 8

MASK 7 = POLY



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(Trench)

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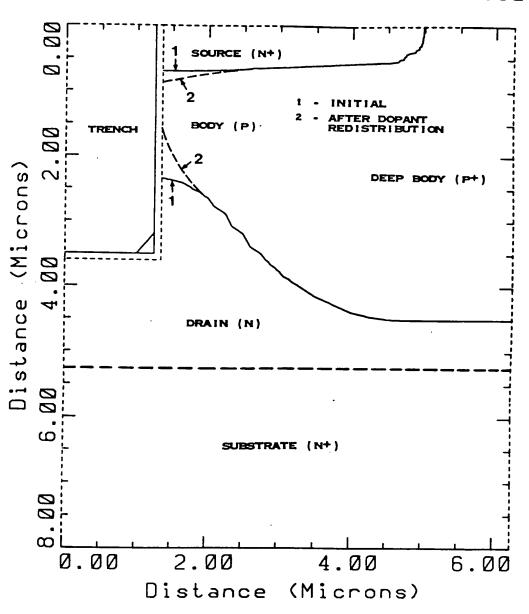
Distance From Trench Boundary

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FIG. 32

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DEVICE, RDSON SIMULATION - G32



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